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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 5

### Complete if Known

Application Number	09/616,385
Filing Date	07/14/2000
First Named Inventor	Enric Musoll
Art Unit	2183
Examiner Name	Eric Coleman
Attorney Docket Number	P3809

### U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
EC		US- 5600837 A *	02-04-1997	Artieri, Alain	
EC		US- 5461722 A *	10-24-1995	Goto, Tatuhiro	
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Examiner  
Signature

*Eric Coleman*

Date  
Considered

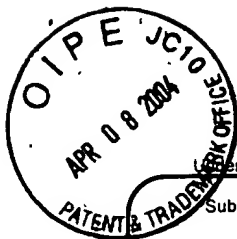
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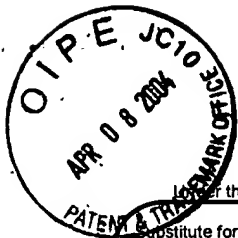
Examiner Signature	<i>Eric Coleman</i>	Date Considered	6/27/04
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		* FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp 210 -221, IEEE	
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		* STEERE et al., "A Feedback - Driven Proportion Allocator for Real-Rate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp 145-158, USENIX Association	
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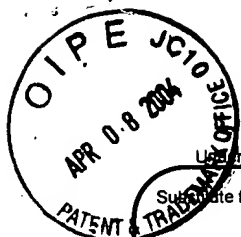
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		* The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition, May 1994, pp 70-72, Morgan Kaufmann, San Francisco	
		* MC68020 32-Bit Microprocessor User's Manual, Third Edition, 1989, pp 3-125, 3-126, and 3-127, Prentice Hall, New Jersey	
		* POTEI, M.J., Real-Time Playback in Animation Systems, Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp 72-77, San Jose, CA	
		* ARM Architecture Reference Manual, 1996, pp. 3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall	
		* ESA/390 Principles of Operation, IBM Library Server, 1993, Table of Contents and Para. 7.5.31 and 7.5.70 (available at : <a href="http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ9AR001/CCONTENTS">http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ9AR001/CCONTENTS</a> )	
		* MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp. 10-66, 10-67 and 10-71, Motorola, Inc.	
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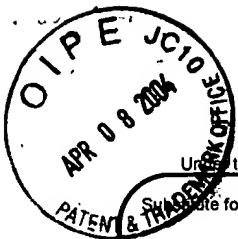
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		* BRADFORD, JEFFREY et al., Efficient Synchronization for Multithreaded Processors, Workshop on Multithreaded Execution, Architecture and Compilation, January-February 1998, pp. 1-4	

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